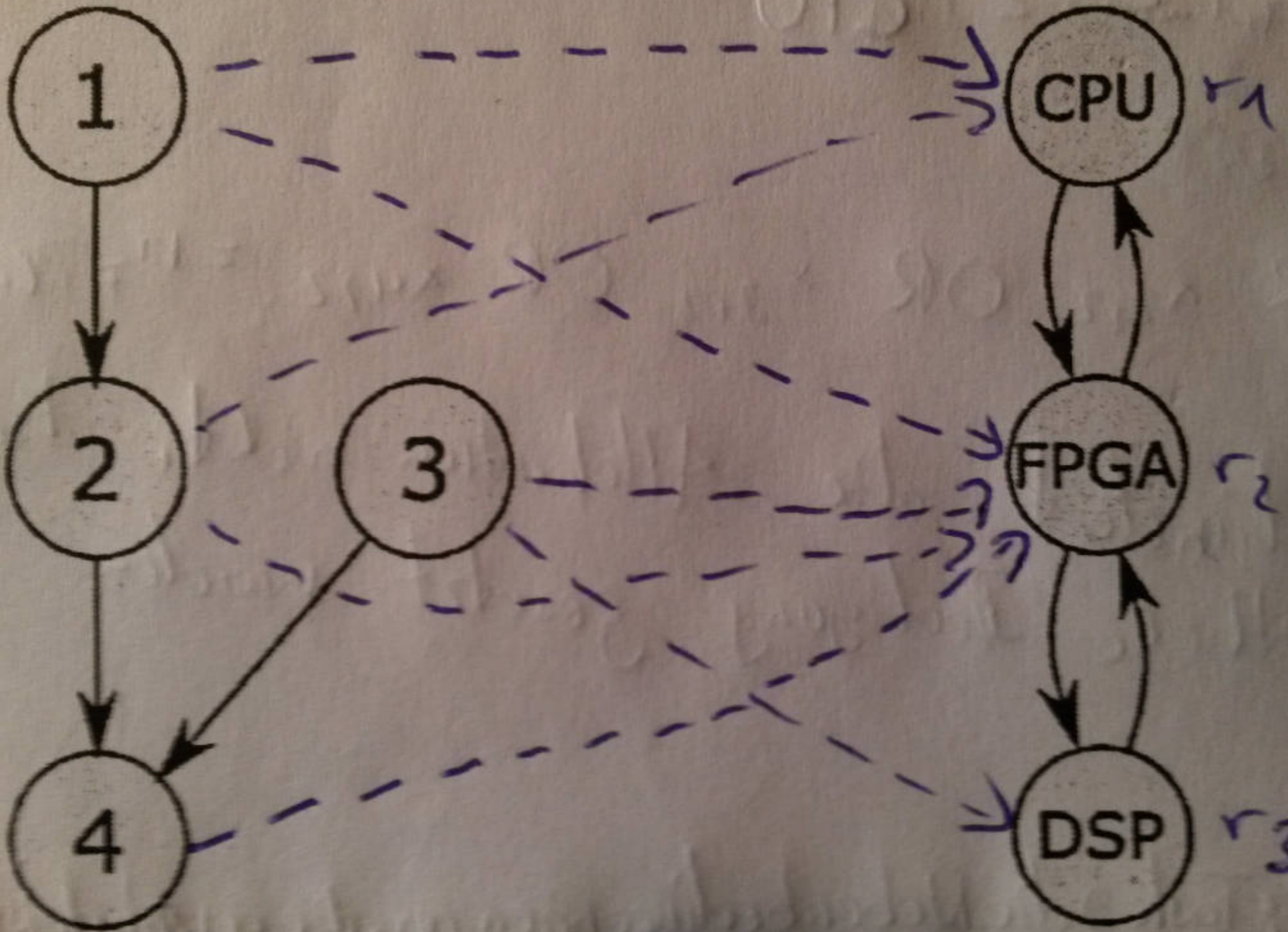
1
2
3
4
CPU
FPGA
DSP
r1
r2
r3